IN THE SPECIFICATION

Please amend paragraph [0007] (page 4) as follows:

[0007] A problem associated with the ~~convention~~ conventional external test procedure described above is that the transmission of instructions, address/data signals and test results between the tester and the selected memory device is slow, thereby requiring a relatively long period of time to perform the wafer sort test. This long test period slows down production, and ultimately increases the cost of the memory devices.

Please amend paragraph [0010] (pages 5-6) as follows:

[0010] In accordance with an embodiment of the present invention, the control circuit of the non-volatile memory device includes a command register and a comparator. After the tester writes the self-test instructions into the configuration array of the memory device, the tester transmits a start command to the command register. In response to the start command, during a first operating phase, the command register addresses the first self-test instruction in the configuration array, and overwrites the start command in the command register with the first self-test instruction. Subsequently, during a second operating phase, the command register performs the self-test instruction, which involves either writing (i.e., programming or erasing) data values to the memory cells of the main array, or reading/comparing data values from the main array. During write operations, predefined data patterns (i.e., all logic 1 values, all logic 0 values, or alternating logic 1 and logic 0 values) are entered into the memory cells of the main memory array. During read/compare operations, the previously written data is read from the main array and transmitted to the comparator of the control circuit, where the read data compared with the

predefined data patterns to detect errors (i.e., defective memory cells). Upon completing each self-test instruction, the control circuit reads a next sequential self-test instruction from the configuration array, writes the self-test instruction in the command register, and then performs the self-test instruction. Execution of the self-test instructions proceeds until ~~and~~ an end test command is written into the command register, at which point the memory device notifies the tester that the self-test process is completed.

Please amend paragraph [0027] (page 10) as follows:

[0027] In accordance with a fourth aspect of the present invention, a data bus 360 is utilized to pass information between data input buffer 324, control circuit 330, column decoder 314, and output controller 328 in accordance with control signals generated by control circuit 330 and transmitted on control bus 338. During the self-test process, data bus 360 is utilized to pass self-test instructions registered in output controller 328 (which are read from configuration array 340) to command register 332 of control circuit 330. Data bus 360 is operated according to ~~know~~ known techniques.

Please amend paragraph [0028] (pages 10-11) as follows:

[0028] In accordance with yet another aspect of the present invention, a method for performing wafer sort on a non-volatile memory device, such as memory device 300, includes writing a series of self-test instructions from a tester to the configuration (first) array 340 of the non-volatile memory device, and then transmitting a start command that causes control circuit ~~350~~ 330 to sequentially read and execute the series of self-test instructions from configuration array 340. Execution of the series of self-test instructions involves

writing at least one data pattern (e.g., 00, 01, 10, or 11) into main array (second memory cells) 310, reading data from main array 311, and then comparing the read data with the data pattern using comparator circuit 334 to detect defective memory cells in main array 311. The self-test method is described in additional detail below with reference to Fig. 5.

Please amend paragraph [0029] (page 11) as follows:

[0029] Referring to the top of Fig. 5, in accordance with ~~know~~ known wafer sort methods, probes are applied to contact pads and power applied (block 510) in a manner similar to that shown in Fig. 1 (described above). Upon power up, memory device 300 performs an optional reset operation (block 515) according to reset program that is, for example, hard-wired into the control circuit 330. In one embodiment, this reset operation includes resetting all registers, power supplies, and configuration bits of memory device 300 to predetermined default values.